An 11.1 Gbps Analog PRML Receiver for Electronic Dispersion Compensation of Fiber Optic Communications

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Abstract—A dispersion tolerant receiver for fiber-optic links, in 0.18 μm SiGe BiCMOS, implements a Class-2 partial response maximum likelihood (PRML) equalization entirely in the analog domain. Post-FEC error free operation is achieved with data received from over 400 Km of uncompensated single mode fiber (SMF). The 4.5 W ASIC operates at up to 11.1 Gb/s and includes a variable gain amplifier (VGA) with automatic gain control (AGC), a 1.5–3.5 GHz programmable continuous-time filter (CTF), a 5-tap sampled-time finite-impulse response (FIR) filter, a decision directed timing recovery, and a 4-state analog Viterbi detector implementation. The receiver is compliant with XFI jitter specifications for Telecom applications (SONET OC-192 and G.709 “OTU-2”).

Index Terms—Continuous-time filter, electronic dispersion compensation, fiber optic, FIR, maximum likelihood detection, OTN, partial response, timing recovery, VGA, Viterbi, WDM.

I. INTRODUCTION

CHROMATIC and polarization mode dispersion in optical fiber causes inter-symbol interference and subsequently leads to errors at the receiving end of the channel. Optical dispersion compensation requires inconvenient and expensive compensation modules commonly placed at 80 Km intervals. Electrical dispersion compensation (EDC) provides for a simple low cost solution by replacing expensive optics with inexpensive electronics. Recently, maximum likelihood sequence estimation (MLSE) techniques have evolved as the preferred approach for high-performance EDC in 10 Gb/s fiber-optic systems [1], [2].

Previously reported EDC receivers employ an analog front-end including a VGA and an ADC followed by a DSP. The reported solutions are either based on a dual-chip or are entirely implemented on a single chip using an advanced CMOS process. They utilize a narrow sliding window for their digital implementation of the Viterbi Decoder resulting in suboptimal performance [2]. In this paper, we present a single-chip small form factor (2.5 mm × 2.5 mm die) solution based on partial-response maximum likelihood (PRML) system in which complex signal-processing algorithms, including the MLSE, are implemented entirely in the analog domain on a mature 0.18 μm SiGe process. Our approach augments the MLSE with partial-response equalization. This kind of multi-stage equalization results in a reduced complexity and a superior performance compared with the MLSE-only approach. Some aspects and blocks of the IC were previously reported [3]–[6], [12]. This presentation aims to show the entire receiver architecture as well as to describe blocks and functions not covered in previous publications such as the MLSE decoder. More details are also added to the descriptions of VGA, CTF, FIR, and CR blocks and their implementation aspects in the context of the fiber optic EDC receiver ASIC.

II. ARCHITECTURE

A. Architecture Overview

A high-level block diagram of the proposed PRML system is illustrated in Fig. 1. Equalization is performed in two steps. In the first step, a partial-response (PR) equalizer shapes the spectrum for the received signal into a predetermined frequency response of a target partial-response signal. In our implementation, the PR equalization is implemented using programmable continuous-time and FIR filters. The output of the FIR block is then applied to the MLSE detector where data recovery takes place. Precise clock and symbol timing are provided by a multi-level decision-directed clock recovery (CR) block.

The simplified block diagram of the IC is shown in Fig. 2. The dispersion impaired optical data signal from the fiber is converted to the electrical domain by a transimpedance amplifier (TIA) and is fed to the 50 Ω terminated VGA for amplitude normalization and then enters a CTF to undergo normalization of the frequency response. A 5-tap discrete time FIR filter provides for further equalization and is responsible for sampling of the signal in a time interleaved fashion subsequently splitting the data stream into two channels (A and B). In the technology chosen (SiGe BiCMOS HBT–150 GHz Ft), analog signal processing and track-and-hold operations at the full line rate of 10 GS/s are prohibitive due to speed, precision, power dissipation, and supply headroom constraints. An interleaved architecture greatly relaxes the most challenging requirements without adversely impacting the overall performance. The Viterbi decoder consists of an add-compare-select (ACS) function and a survival...
sequence register (SSR). A 2:1 MUX assembles the error corrected data back into a single bit stream and ships it out through a 50 Ω terminated buffer. The CR block provides the timing for the FIR, ACS and SSR as well as the synchronization of the other on-chip functions.

The automatic gain control (AGC) loop involving the VGA, peak detectors (PD) and an AGC logic block is responsible for coarse tuning of the CTF output signal swing. When the CR enters the phase locked mode, the AGC control logic switches to the “fine” loop through the PD2 maintaining the signal swing at the FIR (Ch A) output equal to REF2. The VGA gain in the AGC loop is controlled by a 7-bit DAC. An automatic offset correction feature is employed for canceling out of the offset introduced in the VGA and the CTF. An offset control overriding option is implemented in order to provide for external offset control. For example, it allows the forward error correction (FEC) processor to optimize the offset based on the minimum bit error rate. PTAT and bandgap bias currents referenced to internal as well as external resistors are generated for various analog functions. High-speed as well as DC test functions are implemented in order to make possible probing of the signals along the data path as well as DC bias voltages and also temperature in three different on-chip locations.

B. System Link Budget

The aforementioned key building blocks of the ASIC were designed to meet stringent performance requirements. For long-haul fiber optic communication systems, a bit-error rate (BER) of $10^{-4}$ or better is typically required. This BER ensures error-free operation when a FEC such as ITU’s G.709 is employed. To guarantee such a BER performance, a corresponding detection signal-to-noise ratio (SNR) of about 14 dB is required. Assuming without loss of generality that the distortions corrupting the transmitted signal are all independent, stationary processes, a detection SNR may be defined as follows:

$$\text{SNR}_{\text{det}} = \frac{E \{ I_d \}}{\sigma^2_{\text{total}}}$$

where $I_d$ is the desired signal and $\sigma^2_{\text{total}}$ is the total energy contribution from thermal noise, optical link impairments, circuit distortions, and residual mismalization. That is,

$$\sigma^2_{\text{total}} = \sigma^2_{\text{link}} + \sigma^2_{\text{noise}} + \sigma^2_{\text{dist}} + \sigma^2_{\text{miscal}}.$$
The misequalization energy $\sigma^2_{\text{mismatch}}$ is due to the residual intersymbol interference (ISI) left unequalized by the FIR filter. It must be noted that the distortions caused by the link (optical noise, optical nonlinearity) and misequalization produce the dominant terms in (2).

As described above, the received signal undergoes a series of signal processing operations as it travels down the receiver path in the ASIC. While the receiver chain is designed to guarantee error-free (with FEC) data recovery, the circuitry of its building blocks (VGA, CTF, FIR, etc.) corrupts the incoming signal with thermal noise and various circuit distortions. Thus, we may write

$$\sigma_{\text{dist}}^2 = \sigma_{\text{VGA}}^2 + \sigma_{\text{CTF}}^2 + \sigma_{\text{FIR}}^2 + \sigma_{\text{ACS}}^2 \cdots$$
$$\sigma_{\text{noise}}^2 = \sigma_{\text{VGA},n}^2 + \sigma_{\text{CTF},n}^2 + \sigma_{\text{FIR},n}^2 + \sigma_{\text{ACS},n}^2 + \cdots$$

(3)

For a 400 Km reach, optical SNRs (inversely proportional to $\sigma_{\text{link}}^2$) of better than 20 dB are typical. Distortion due to misequalization is a function primarily of the number of taps in the FIR filter and the link reach. For a 5-tap FIR and a 400 Km single-mode fiber link, the equivalent misequalization SNR is found experimentally to be around 20 dB. In order to meet the required detection SNR of 14 dB, (1)–(3) can be used to estimate minimum signal-to-noise-and-distortion ratios (SNDR) for each block in the ASIC receiver chain. In our setup, a 29 dB SNDR for each block in the ASIC receiver chain, is found to be adequate for error-free data recovery (with FEC).

III. CIRCUIT DESCRIPTION AND MEASUREMENTS

A. VGA/AGC

An input signal coming from a TIA may vary from 160 mV to 780 mV in this application. A linear VGA (Fig. 3) is implemented as a part of a dual loop AGC normalizing the signal amplitude at the FIR input (coarse loop) and at the FIR output (fine loop). The requirements for the AGC include the minimum gain adjustment range from $-8$ dB to $+4$ dB. The required 29 dB SNDR at the CTF output takes into account the signal degradation resulting from both distortion and noise. Assuming equal contributions of noise and distortion, the required VGA/CFI’s combined SNR has to be above 33 dB. In order to prevent the VGA from limiting the VGA/CTF’s output SNR, the VGA’s SNR has to remain above 40 dB or 0.88 mV RMS at the 250 mV_{IPK-IPK} output. The VGA gain is controlled by a current from a 7-bit DAC. Thermometer coding is used in the DAC in order to ensure monotonic transfer characteristic for avoiding of the AGC loop malfunction. The DAC is controlled by the AGC logic (AGCL) block which functions according to a special algorithm. The AGCL consists of a finite state machine controller and a 7-bit synchronous counter. The AGCL samples the amplitude error information from both loops and drives the VGA gain until this error is zero. The AGC amplitude error is a difference between the CTF/FIR output peaks or amplitudes and an ideal voltage reference that represents the desired signal level. The output of the CTF (coarse loop) and the output of the FIR (fine loop) are sent to the corresponding peak detectors. The peak value of these signals is compared differentially to the AGC reference voltage, which is programmable via a 7-bit linear DAC. The analog amplitude error drives a 1-bit ADC. The output of the ADC is synchronized to the AGC system clock and drives the digital controller. The gain control loops are working one at a time. The coarse loop lock is achieved first. It ensures that a 900 mVpp swing data signal enters the FIR. This corresponds to about 250 mV_{IPK-IPK} at the CTF input. Once the CR achieves a lock condition, the coarse loop is switched off transferring the control to the fine loop for continued monitoring and fine adjustment of the data signal swing at the output of the FIR. The fine AGC loop ensures that a 900 mVpp signal swing is delivered to ACS. The fine loop is also responsible for the accommodation of any deviations of the signal level at the output of TIA during the operation of the IC. The automatic offset control block cancels out any offset in the signal chain along VGA and the CTF. A Gm-C based loop filter instead of an RC filter is used for setting the low frequency response of the automatic offset control, since the implementation of the Gm cell requires much less on-chip area compared to Mega-Ohms of resistance necessary for the low cut-off frequency. Moreover, Gm in contrast to R can be set virtually independent on process corners. This is achieved by deriving the Gm cell bias current using an external resistor. The current consumption of the Gm cell in the Gm-C based loop filter is below 100 $\mu$A. Since the Gm cell is balanced during normal operation, the linearity is not an issue. Temperature dependence is eliminated by using PTAT bias current. 100 Hz low cut-off frequency is achieved. The cut-off frequency remains within $\pm 25\%$ over process, voltage and temperature (PVT) variation. Capacitance variation over process corners contributes the most to the cut-off frequency variation. The offset control voltage on the capacitor is converted to current by another Gm cell which is subsequently inserted into the VGA output termination point. This ensures the offset control loop bandwidth independence on the VGA gain. The automatic offset control can be disabled for external digital control of the offset through the 7-bit DAC.

B. CTF

Fig. 4 shows a block diagram of the fourth-order Gm-C low-pass CTF. It consists of two biQuads, the input voltage-to-current converter and the output current-to-voltage converter. A three biQuad version of the filter (the sixth order) has previously been described in detail [4]. This CTF features 230 mW—significantly lower power compared to the reported sixth-order CTF. The biQuad’s power consumption is 69 mW. The biQuad (Fig. 4) transfer characteristic is:

$$H(s) = \left(g_{m1}V_{IN} \cdot g_{m2}\right) / \left(C^2 \cdot s^2 + g_{m3} \cdot C \cdot s + g_{m1} \cdot g_{m2}\right).$$

Component values are calculated by equating the biQuad’s transfer characteristic to a normalized second-order low-pass filter equation with Bessel coefficients to ensure the linear phase. Cascading two biQuads provides the fourth-order response and extends the linear phase beyond the cut-off frequency point. The CTF cut-off frequency as measured can be tuned from 1.5 to 3.5 GHz with 4-bit granularity through a digital serial interface. The tuning range is sufficient to accommodate the incoming data rates ranging from 9.953 Gb/s to 11.1 Gb/s that require the CTF’s cut-off frequencies to be from 1.8 to 2.5 GHz.
Additional 4-bit cut-off frequency tuning capability is built-in for the compensation of the impact on the cut-off frequency of the PVT variation. Simulated BW over the PVT is as follows: 0.9 to 1.5 GHz ($C = \max$, $g_m = \min$) and 3.5 to 5.4 GHz ($C = \min$, $g_m = \max$). The CTF group delay was measured to be flat to $\pm 10$ ps up to 1.2 times the BW. In simulation over the PVT, however, the group delay variation did not exceed $\pm 5$ ps. THD was measured to be below $-40$ dBc at 500 MHz frequency. The required minimum SNDR at the CTF’s output is 29 dB. We have achieved the required SNDR for the worst PVT corner in simulation with the VGA included in the signal path. Simulated VGA/CTF combined SNR is 33 dB with the CTF being the main noise contributor. The most critical component in CTF is a linearized OTA. The requirement of achieving high frequency at reasonable power limits the OTA’s architecture to the simplest diff-pair and rules out the possibility of the application of the CMOS transistors. The SNR requirements dictate the CTF ability to work with as large signals as possible. The increase in signal levels causes $g_m$ degradation resulting in compression as well as change in CTF bandwidth and group delay characteristics. There are several methods that require resistors for the purpose of increasing the dynamic range of a diff-pair [4]. It leads, however, to $g_m$ varying over process corners resulting from resistance variation. In our application, a cross-connected diff-pair ratioed as 1:5 is found to produce best linearity results (Fig. 5).

**C. Current Reference Circuits**

In general, on-chip resistance may vary over process corners more than 25% while $g_m$ can be set virtually independent of PVT variation. For this reason, it is preferable to rely on $g_m$ rather than on resistance when setting the cut-off frequency in the offset control circuit and, more importantly, in the OTAs used in the CTF. $g_m$ simulated for the proposed OTA (Fig. 5) and for the OTA linearized by using an emitter degeneration resistor is presented in Fig. 6. Resulting $g_m$ variation over process corners for the proposed OTA [Fig. 6(b)] shows much less $g_m$ variation compared to the emitter degenerated OTA [Fig. 6(b)]. Temperature dependence of $g_m$ [Fig. 6(c) and (d)] is decreased by using the PTAT bias current. The schematic diagram of the PTAT reference producing currents proportional to both $1/R_{int}$ and $1/R_{ext}$ is shown in Fig. 7.

To establish the constant over temperature bias voltage, the bandgap current reference has to be proportional to $1/R_{int}$ since the bias voltages are setup by passing the current through internal resistors. The bandgap current reference circuit used in this design is shown in Fig. 8.

**D. FIR Filter**

Equalizers such as a FIR filter are used in fiber optics to transform the severely distorted NRZ data into a predictable pre-defined target signal that allows for robust clock and data recovery. There are several key features of the FIR block needed
Fig. 6. $g_m$ simulated for an OTA linearized using an emitter degeneration resistor (a), (c) and for the proposed (Fig. 5) OTA (b), (d). $g_m$ variation over process is presented in graphs (a) and (b) and variation over temperature in graphs (c) and (d).

Fig. 7. Schematics of the current reference producing both PTAT currents proportional to $1/R_{\text{int}}$ and to $1/R_{\text{ext}}$.

Fig. 8. Schematic diagram of the current reference block producing the bandgap current proportional to $1/R_{\text{int}}$.

for this application. An improved wideband track-and-hold (T/H) topology is implemented to achieve high speed and resolution at low power levels. A wideband, fast-settling, linear current summing node minimizes distortions in the signal path. The FIR filter DC power dissipation is 900 mW from a 3.3 V supply.

Fig. 9 shows an overall block diagram of the functionality of the 5-tap FIR filter. On the EDC IC, the VGA and CTF precede the FIR, and these circuits provide gain and equalization of the input signal so the optimum signal swing is presented to the FIR block. The FIR filter provides further equalization of the signal. For a 10 Gb/s application, an interleaved structure results in a 5 GS/s operation for each T/H in the chain and a sampling clock that is 180 degrees out-of-phase for each T/H bank. Each tap coefficient is generated through a DAC, and a Gilbert cell is used to multiply the signal by the digitally programmed tap weight. The outputs of the Gilbert cells are current mode signals that are summed together to drive the output T/Hs. Each of the interleaved filter outputs has a digitally controlled offset voltage to optimize the signal as a function of the optical reach. For proper operation of the FIR filter at high sample rates, the clock skew between the first T/Hs must be controlled to < 1 ps. This requires careful layout considerations and extracted simulations.

Conventional high-speed Si bipolar T/H designs [13] typically are based on a supply voltage of at least 5 V and relaxed power dissipation requirements. The 3.3 V supply and stringent
power dissipation requirements in this design forced us to introduce new design techniques to guarantee the required precision and speed over PVT. The T/H in [13] dissipates 700 mW whereas the T/H in this paper draws 30 mW off a 3.3 V supply. This represents a power reduction of greater than one magnitude with comparable distortion performance.

Fig. 10 is the schematic of the improved T/H design. The standard switched emitter follower (SEF) based T/H architecture [7] has been enhanced by the addition of an isolation buffer stage from the output of the $G_M$ stage to the SEF input. The isolation buffer consists of transistors $Q_2P$, $Q_2N$, DP, and DN and resistors $R_{DP}$ and $R_{DN}$. In track mode, the buffer provides a zero volt level shift, and the output impedance is significantly lower than previous implementations, where the $G_M$ stage, with the high output impedance, provides a poor drive capability at high frequencies. The low output impedance feature of the buffer in the new T/H provides enhanced drive capability for the SEF and feed-forward capacitors, which results in improved track mode acquisition settling time. This is accomplished without the need for increased power dissipation. In hold mode, the transistors DP and DN are reverse-biased due to the differential pair current $I_{sw}$ into $R_{DP}$ and $R_{DN}$. The resultant hold mode isolation provides reduced feed-through as compared to the previous approach. This is a consequence of the reverse-bias voltage on the CJE of the SEF transistors $Q_3P$ and $Q_3N$. The differential T/H circuit dissipates 30 mW on a 3.3 V power supply. The performance of the T/H was simulated under various conditions to determine the anticipated dynamic range. The simulated track mode bandwidth (BW) of the T/H is 22 GHz. The third harmonic distortion (HD3) for the differential T/H was simulated under Nyquist conditions, at 5 GS/s and 10 GS/s, with 1 V peak-to-peak (pp) input signal. The simulated sampled mode HD3 performance was 54 dBc and 43 dBc (the measured THD for a 3 GHz signal for the T/H in [13] appears to be comparable to the HD3 performance for a single T/H in this work), respectively, assuming no mismatch between the (+) and (−) channels of the T/H. Based on a linearity of 54 dBc per stage for a single T/H, the overall HD3 is 42 dBc for the cascaded 5-stage T/H chain (see [6] for a comparison of state-of-the-art T/Hs with our proposed topology).

Fig. 11 shows the schematic of the summing nodes that are driven by Gilbert-cell multipliers (Fig. 9). The digitally con-
trolled tap coefficient scales the output signal from each T/H. The output of each Gilbert cell drives a transconductance amplifier. The cascodes QC1 and QC2 sum the output currents of the transconductance amplifiers, and the output drive the final T/Hs (Fig. 9).

Fig. 12 shows the test setup for the characterization of the FIR. The feed-through of the VGA-CTF-FIR chain is measured with the tap coefficients set so that all the Gilbert cells are balanced, and the FIR input is isolated from the FIR output. The input data from the signal generator is 11.1 Gb/s, PRBS-31 NRZ signal, with a coherent tone at 0 dBm. The measurement of the coherent tone at the test buffer is 40.8 dBm. The test buffer differential-to-single-ended gain is 0.45 (6.9 dB), which produces 33.9 dBm at the FIR output. The noise floor of the T/H block was simulated and correlated to measurement. The simulated sampled mode RMS noise for a single T/H is 3.2 mV at the measured junction temperature. A high-speed sampling oscilloscope, referred to here as the DCA, is used to measure the RMS noise of the output T/H (Fig. 9) with all the FIR tap coefficients set to zero. This allows the dominant noise source of the signal path to be the output T/H. The measured RMS noise is 1.7 mV at the single-ended output of the test buffer. The test buffer gain is 0.45, which results in a T/H differential noise 3.4 mV, which agrees well with simulation. The FIR tap delay, from tap #1 output to tap #5 output, is measured to be 401.9 ps, compared to an ideal value of 400 ps. The tap-to-tap delay is approximately 100 ps (i.e., the symbol period for a 10 Gb/s second signal). The FIR gain is measured at each of the 5 taps, for all of the 7-bit DAC codes. From the measured gain transfer function in Fig. 12, it can be seen that the FIR tap gain is a linear function of the DAC codes.

E. Clock Recovery

The proposed multilevel CR uses a decision-directed algorithm based on the minimum mean-squared-error criterion [5], [8]. Its basic block diagram is shown in Fig. 13. Simply stated, the timing information is obtained as the instantaneous gradient, with respect to phase of an error signal that is proportional to the phase. Suppose the received signal $y_k$ is produced by sampling the continuous signal $y(t)$ at instant $t = kT + \tau$, where $T$ is the symbol period and $\tau$ represents a timing offset. In timing recovery algorithms based on the mean-squared-error (MSE) criterion [9], the sampling clock phase is adjusted such that the MSE

$$E\{e_k^2\} = E\{(x_k - y_k(\tau))^2\} \quad (4)$$

is minimized. This optimization results in the following phase estimate signal:

$$z_k = e_k(y_{k+1} - y_{k-1}). \quad (5)$$

The phase estimator based on (5) is depicted in Fig. 14. In our implementation, the timing recovery block operates on a signal that has been equalized to an ideal class-2 partial-response (PR2) signal. In practice, the ideal PR2 signal, $x_k$, in
(4) is not available but an estimate based on its quantized value may be obtained. The phase estimate signal \( z_k \) is then fed into a PLL loop that adjusts the frequency of a voltage-controlled oscillator (VCO). Initially, a traditional PLL, with a phase-frequency detector (PFD), is used to lock the frequency of the VCO to the incoming data rate. The VCO and loop filter are initially set to an internal common-mode voltage (CMV) for coarse frequency tuning and then released to a type-2 charge pump PLL. Once frequency lock is achieved, the control of the VCO is transferred to a decision-directed phase detector (DDPD) phase alignment loop which is using the incoming data stream as reference. The DDPD loop minimizes the minimum-mean-square error (MMSE) between the incoming data and the ideal \((1 + D)^2\) PR2 polynomial. The transition from frequency acquisition mode to phase alignment mode is automatically controlled by a finite-state-machine, namely, the lock-detect (LD). Once the LD has been initialized with a reset, the LD will automatically control the dual-loop CR. The CR loop drives the FIR and the Viterbi decoder clock inputs maintaining an optimal sampling phase.

The performance, in terms of jitter tolerance, transfer, and generation of the proposed CR block Jitter Tolerance were assessed using JDSU ONT-506 tester. Jitter tolerance results shown in Fig. 15(e), indicate that the CR block is compliant with the SONET jitter tolerance mask. Jitter transfer and generation results are illustrated in Fig. 15(d). For a system bandwidth setting of 8.0 MHz, the measured bandwidth shown in Fig. 15(d) was found to be around 7.6 MHz with a corresponding jitter generation of 6.4 mUI\text{rms} and a jitter peaking of 0.01 dB. For a system BW setting of 3.6 MHz, The measured bandwidth and generation were found to be around 2.3 MHz and 4.9 mUI\text{rms}, respectively.

\textbf{F. MLSE Decoder}

User symbols recovery is achieved using a four-state MLSE detector. The most likely sequence is determined via the iterative Viterbi algorithm. Accordingly, a trellis is created for the received signal where each trellis branch is “weighted” by a metric proportional to the distance between received and ideal symbols. The most likely sequence is the “shortest” path through trellis. The metrics and paths are stored in memory whose size depends on the trellis depth. Typically a trellis depth of at least 5 times the channel memory is used for robust data recovery.

An example trellis of our four-state MLSE is illustrated in Fig. 16. The trellis was generated using a \([-1 -1 1 1 -1 1 1 1]\) sequence for system SNR of 17.9 dB. The cumulative metrics are shown at the end of the trellis. Also shown are the corresponding input/output symbols for each branch in the trellis. The optimal path, having the least metric, through the trellis is highlighted in red. The most likely sequence is recovered by backtracking the optimal path.

The Viterbi decoder consists of ACS function, where metrics computations is performed, and a SSR where backtracking of the optimal path takes place.
In our implementation, the interleaved discrete-time analog ACS block is optimized for a \((1 + D)^2\) PR target that is obtained by applying partial-response equalization on the original binary sequence. The basic architecture of the ACS block is depicted in Fig. 17. The two five-level equalized input signals from the FIR filter channels A and B are retimed in two track and hold circuits and distributed to the ACS core slices as well as to unity gain linear output buffers connecting to the phase detector block in the CR. Each slice contains an interleaved version of the metric update circuitry, the metric track-and-hold and additional support circuits. The challenge of the non-windowed non-unrolled-loop branch/path metric calculation is the constraint of the extremely short cycle time of under 80 ps. From a system point of view, the ACS metrics update equations are uniquely arranged to allow the circuit implementation to achieve the maximum circuit symmetry paired with the maximum SNR at the digital decision circuits. This is vital for achieving the high equivalent input SNR and low bit error rates. The performance of the ACS block is determined by the accuracy of the internal metric update calculation and the accuracy of the equalization in the CTF/FIR front-end to match the optimum five-level target. For the ACS, the 29 dB SNDR requirement translates into a computational accuracy for a single metric circuit of better than 5 mVrms.

A 2 × 4-channel digital output of the ACS bus connects to the SSR (Fig. 18) channels: interleave A and B. The SSR block chooses the final survivor based on a majority vote calculation at the end of the SSR chain. The building block of the SSR is a multiplexed latch depicted in Fig. 19. The latch is clocked using a multiphase clocking scheme gated by a select switch. The SSR block contains a total of 160 such cells. The interleaved channels are finally combined in a 2:1 MUX circuit and fed into an XFI compliant output buffer. All SSR clocking is implemented at half-rate. As a result, the residual offset and/or duty cycle distortion in the clock signal driving the output 2:1 MUX can cause even–odd bit duty cycle distortion. Special care was taken to mitigate this effect by providing careful offset compensation for clock driver circuitry.

G. Test Points

The high complexity of this analog receiver makes it difficult to assess the operation of the functional blocks and to identify potential problems in the circuits. High-speed test point (TP)
circuits are introduced for probing the signals. The use of TP makes it possible to pick up the high speed data signals at the critical points along the signal path with minimal loading of the precision-analog circuits and minimal perturbation of the layout integrity (Fig. 20).

A high-speed signal is picked up by a probe that has a driving capability to transmit the signal to the periphery of the block (≤50 μm). A line driver picks up the signal from the probe and transmits it over larger distance (≤1 mm). An analog MUX selects one out of up to seven high-speed signals coming from the line drivers and ships them to the output through a 50 Ω terminated linear buffer. The DC voltages of the critical biasing points, the voltage drop on ground plane and power supply as well as voltages corresponding to the on-chip temperature are routed out through an integrated DC test point. Since the DC test point is bidirectional it also provides the capability of adding or subtracting of currents to/from a specific point in the circuit.
Fig. 17. Viterbi decoder ACS block diagram.

Fig. 18. Viterbi decoder SSR block.

Fig. 19. SSR MUXed latch stage.
IV. IC LAYOUT AND FABRICATION

Since frontend of the ASIC implements a precision analog function, special attention is paid to the design of CTF layout. The layout (Fig. 21) is made as compact as possible along the direction of the signal path by seeking to reduce the capacitive and resistive parasitics on sensitive high speed signal nodes. Control and biasing circuits are moved away from the signal path and are laid out less tightly. In order to ensure the ratioed diff-pair is well-balanced, particular attention is paid to its layout design. Due to the fact that there are 12 signal transistors and four current sources (Fig. 5), the layout of the cell is relatively large. Consequently, it is evident that the regular symmetrical layout would space the components apart, thus compromising the symmetry in case of the process parameters and temperature gradients. To avoid this effect, the transistors in the diff-pairs are interdigitated and placed in two rows (Fig. 22). The current source transistors and resistors are placed at the edges of the layout, namely, \( I_{E1}, I_{E2} \) are located on one side and \( I_{E12}, I_{E21} \) are placed on the other.

The Jazz Semiconductor 0.18 \( \mu m \) SiGe process featuring 150 GHz/200 GHz \( F_t/F_{\text{max}} \) is used for the IC implementation. The die size is 2.5 mm \( \times \) 2.5 mm (Fig. 23) with the VGA occupying 0.15 mm\(^2\), CTF 0.17 mm\(^2\), FIR 0.21 mm\(^2\), CR 0.68 mm\(^2\), ACS 0.55 mm\(^2\), SSR 0.14 mm\(^2\). The test chip is wire-bonded in a custom ceramic BGA package and consumes 4.5 W from 3.3 V, 1.8 V and \(-1.2\) V supplies with VGA consuming 0.06 W, CTF-0.23 W, FIR-0.9 W, ACS-2.2 W, CR-0.79 W and SSR-0.32 W.

V. OPTICAL SYSTEM TEST RESULTS

To assess the performance of the PRML EDC receiver IC, a 10.71 Gb/s, \( 2^{31} - 1 \) PRBS NRZ data is launched onto an uncompensated \( 5 \times 80 \) Km-span SMF fiber link. A standard Mach–Zehnder modulator is used. The light source is a 1550 nm wavelength laser, and the link consists of four Erbium-doped fiber amplifiers spaced at 80 Km. An optical bandpass filter precedes a standard linear PIN-TIA receiver. Typical optical powers at the receiver are in the range of \(-6\) dBm to \(-18\) dBm (or even as low as \(-24\) dBm with an APD receiver). The corresponding TIA differential peak-peak amplitude typically ranges from 30 mV to 250 mV. A bit-error rate tester was used to detect errors and generate the NRZ data signal. The test setup is shown in Fig. 24. Fig. 25 depicts the received eye after a transmission distance of 400 Km (a), the equalized eye at the FIR output (b) and the recovered clock and data eye at the IC output (c). As can be seen, the received eye is totally closed. The PR2 equalization has produced the expected \((1+D)^2\), five-level eye (with residual misequalization) which is then applied to the four-state MLSE for NRZ data recovery. OSNR-versus-reach results are depicted in Fig. 26. The required OSNRs for a back-to-back setup and over a 400 Km link of standard-mode fiber are found to be around 16 dB and 25 dB, respectively. The required OSNR increases at a slope of less than 1.5 dB/80-Km-span (or 1.5
VI. CONCLUSION

The PRML receiver presented here is capable of post-FEC error-free recovery of up to 11.1 Gb/s data transmitted over 400 Km of uncompensated SMF fiber. In contrast to existing MLSE receivers that fully rely on a digital Viterbi decoder, our
architecture is entirely analog. The realized reach of this receiver exceeds that of any reported EDC receiver employing standard NRZ transmission and direct detection (non-coherent, IM-DD) means (Table I). The outstanding performance of this PRML receiver has been achieved with a one-sample/bit, four-state MLSE [3]. This EDC receiver shifts optical transmission issues from the optical domain to a low cost IC solution. To the best of our knowledge this is the first reported analog implementation of the PRML algorithm for a 10 Gb/s fiber-optic receiver.

REFERENCES


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Harry Tan has over 30 years of experience in communications system and network design and analysis. Prior to co-founding Menara Networks as its Chief Scientist, he was the co-founder and CTO of Qplus Networks, a start-up engaged in the development of ultra-long haul 40 G fiber optic WDM transport systems employing phase modulation. He also brings over 25 years of experience as an Electrical Engineering faculty member at Princeton University and at the University of California, Irvine. He has taught and performed research in information theory and coding, digital modulation, data compression, optical communications, high speed routing protocols and wireless data networking protocols and has authored over 70 peer reviewed publications. He has also served as a consultant to the Jet Propulsion Laboratories and to The Aerospace Corporation as well as other technology companies. He received the SB degree in EE from the Massachusetts Institute of Technology and the MS and Ph.D. degrees in engineering from the University of California, Los Angeles and is a member of Sigma Xi, Tau Beta Pi and Eta Kappa Nu.

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